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AF/2823

IR-1444 DIV (2-2480)

THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF APPEALS AND INTERFERENCES

In re Patent Application of
Milton J. Boden, Jr. et al.
Serial No.: 09/691,083
Filed: October 18, 2000

New York, New York
Date: March 10, 2006
Group Art Unit: 2823
Examiner: G.R. Fourson III

For: P CHANNEL RADHARD DEVICE WITH BORON DIFFUSED P-TYPE POLYSILICON GATE

Mail Stop: Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO NOTIFICATION OF NON-COMPLIANT APPEAL BRIEF

Sir:

Applicant responds herein to the notice of Notification of Non-Compliant Appeal Brief dated February 10, 2006 (The Notification).

The Applicant has enclosed a revised brief which now includes an Evidence Appendix and a Related Proceedings Appendix prepared according to the Examiner's suggestion.

The Notification further alleges that the Appeal Brief is defective because "the arguments and statements of the grounds of rejection do not address the pending rejection of record based on Wolf, Vol. 1, but is instead directed to the rejection in the office action mailed 11/2/04."

It is presumed that the "pending rejection of record" refers to the paper mailed on July 25, 2005. In that paper, it is stated "The finality of the office action mailed 11/2/04 is withdrawn to correctly indicate the reliance on Wolf, Vol. 1, pp. 207-210. A copy was previously provided but cited as Wolf, Vol. 2 on the PTO-892 mailed 4/29/04." See Page 2, Par. 1.

As recognized by the Examiner in the July 25th Office Action the only difference between the final rejection dated November 2, 2004 and the Office Action dated July 25, 2005, is that Wolf was mis-cited. That is, there is no substantive difference between the two Office Actions. Therefore, the arguments in the Appeal Brief as presented take into account the teaching of Wolf, Vol. 1. The Appeal Brief makes it clear that the cited portions of Wolf were taken into account. For example, the Appeal Brief, page 5, next to the last paragraph, refers to Wolf, pp. 207-210, and also

discusses the same on page 7, second paragraph. Therefore, it isn't correct to state that the Appeal Brief is defective for failing to address Wolf.

Furthermore, the mis-citation of Wolf has been admitted as an error by the Examiner. The Examiner attempted to correct this error by withdrawing the Final Rejection dated November 2, 2004 and re-opening prosecution in the action dated July 25, 2005. No new ground of rejection was asserted in the July 25th Office Action.

In a telephone interview on October 26, 2005 with the Examiner's supervisor, Examiner Matthew Smith, SPE, it was settled that the Office Action of July 25, 2005 was issued in error. The Examiner's supervisor then suggested the filing of a request for the reinstatement of appeal.

In the paper mailed to the Office on November18, 2005, the reinstatement of appeal was requested on the grounds that the re-opening of prosecution was not permitted under the Patent Office rules without a new ground of rejection. The Examiner appears to have recognized the validity of the position taken in the paper dated November 18, 2005 in that he has reviewed the Appeal Brief for submission to the Board. However, in the Notification, the Examiner has asserted that the Appeal Brief is defective because it addresses the Final Rejection dated November 2, 2004, and not the July 25th Office Action.

The Appeal Brief is proper in that it was taken from a Notice of Appeal filed according to the Patent Office Rules from the Final Rejection dated November 2, 2004.

To modify the Appeal Brief to address the Office Action dated July 25, 2005, as directed by the Examiner, would be improper because:

a) the July 25, 2005 Office Action was improperly issued;

b) there is no Notice of Appeal from the July 25th Office Action as is required by the Patent Office Rules (Rule 41.31(a)) before an appeal brief is filed. Regarding the latter, note that in the interview with the Examiner's supervisor it was agreed that the Applicants should not pursue an appeal under Rule 41.31(a) in that such a course of action would require the filing of another notice of appeal. It was agreed that the applicants should not bear the cost of another notice of appeal nor should a hearing on the Applicants' appeal be delayed because the Office Action dated July 25, 2005 was issued in error.

In view of the foregoing, the proper action is the reinstatement of appeal taken form the Final Rejection dated November 11, 2004. The Examiner can note the mis-citation in the answer to the Appeal Brief.

It is respectfully submitted that the new rules relating to the appeal were intended to speed up the resolution of appeals. So far, however, the appeal has been delayed due to errors, which could have been avoided had the rules been followed properly. The delay has cost the applicants patent term, which should be restored.

Prompt consideration of the Appeal Brief on its merits is earnestly solicited.

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DOROTHY JENKINS
Name of Person Mailing Correspondence

Dorothy Jenkins
Signature

March 10, 2006
Date of Signature

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IR-1444 DIV (2-2480)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF APPEALS AND INTERFERENCES

In re Patent Application of	New York, New York
Milton J. Boden, Jr. et al.	Date: March 10, 2006
Serial No.: 09/691,083	Group Art Unit: 2823
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APPEAL BRIEF PURSUANT TO 37 C.F.R. §41.37

Sir:

This appeal is from the Examiner's final rejection of this application dated November 2, 2004.

I. REAL PARTY IN INTEREST

The real party in interest in the above-identified application is:

International Rectifier Corporation
233 Kansas Street
El Segundo, California 90245

II. RELATED APPEALS AND INTERFERENCES

The applicant(s), the assignee(s) and the undersigned attorneys are not aware of any related appeals and interferences.

III. STATUS OF CLAIMS

Claims 1, 3-7, 9 and 11-13 are pending and on appeal herein.

Claims 2, 8, 10 and 14-31 have previously been canceled.

IV. STATUS OF AMENDMENTS

No amendments have been submitted since the Final Rejection dated November 2, 2004.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention is related to a type of MOSgated power semiconductor device typically referred to as radiation hardened. Such a device includes a gate oxide formed to resist damage due to radiation.

A device according to the present invention includes a radiation hardened gate oxide that is less than 1000 Å. The radiation hardened gate oxide in a device according the present invention is unique in that it can withstand damage according to the most well known types of radiation.

To understand the present invention the following background may be helpful. Conventional power MOSgated devices that are used in high radiation environments, such as in outer space, can be damaged if subjected to ionizing radiation or a heavy ion strike. The effects of ionizing radiation can accumulate over time, resulting in device degradation. Also, a single heavy ion strike can lead to catastrophic failure, which is sometimes referred to as single event effect or SEE. MOSgated power devices are particularly susceptible to these problems because of their large depletion volumes and large device areas. Specification at page 1, line 17 - page 2, line 3.

Radiation hardened power MOSFETs, and other MOS gated devices designed for use in space or other high radiation environments have the conflicting design requirements of resisting damage caused by high doses of ionizing radiation on the one hand and of resisting damage due to SEE. Specifically, a thin gate oxide is desired to resist high radiation (megarad) environments, while a relatively thick gate oxide is desired to prevent SEE effects. Specification at page 2, line 14, page 3, line 4.

More specifically, it is known that after exposure to a large total dose of ionizing radiation a positive charge will build up in or at the gate oxide, which causes a shift in the threshold voltage of the device. Further, there is an increase of interface traps at the silicon/gate oxide boundary. Conventional thinking is that both of these effects are reduced by using a

thinner gate oxide, for example, one having a thickness of less than about 900Å. Specification at page 2, lines 14-21.

When a charged particle passes into or through the silicon body of a MOSgated device it generates a large number of electron-hole pairs in the depletion region of the device some of which gather at the gate oxide, resulting in a high potential across the gate oxide. This is the SEE that degrades a device. To prevent failure due to SEE the conventional solution was a gate oxide thicker than about 1300Å. Specification at page 2, lines 22 - page 3, line 4.

Contrary to the conventional thinking, however, the inventors have discovered that a P channel power MOSFET having a radiation hardened gate oxide that is less than 1000Å, specification at page 11, lines 14-15, thick can maintain a predetermined threshold voltage (i.e. resist voltage shift) at a high total irradiation dose, and also maintain SEE withstand capability. Specification at page 17, line 22 - page 18, line 3. That is, it was generally understood that to obtain sufficient resistance to damage due to SEE the gate oxide must be made at least thicker than 1300 Å. See specification at page 2, line 22, page 3, line 4. However, as demonstrated by the data in the application, (see specification at page 17, line 3 to page 18, line 3; see also Figure 14) a device according to the present invention is capable of withstanding damage due to SEE, despite having a thinner than 1300 Å gate oxide.

Claim 1, therefore, calls for the following combination of features:

1. A P-channel MOS gated device which is resistant to single event radiation failure and having improved total dose radiation resistance; said device comprising:

a P-type substrate having substantially flat, parallel upper and lower surfaces;

a plurality of laterally spaced N-type body regions extending from said upper surface into said substrate;

at least one respective P-type source region formed in each of said body regions in said upper surface of said substrate and defining a respective channel region in said upper surface in said N-type body region;

a gate electrode comprised of p-type polysilicon disposed atop and insulated from said channel region and operable to invert said channel region in response to the

application of a suitable gate voltage to said gate electrode said gate being insulated from said channel region by a gate oxide layer comprising silicon dioxide, said gate oxide layer being comprised of radiation hardened silicon dioxide and less than 1000Å thick; and

a source electrode disposed atop said upper surface and connected to said at least one P-type source region;

wherein said gate oxide is capable of resisting threshold voltage shift due to total radiation dose and capable of resisting single event gate rupture due to a single event effect.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claim 1, 3-7, 9 and 11-13 have been rejected as obvious under 35 U.S.C. § 103(a) over Williams, U.S. Patent No. 5,248,627, in view of Kalnitsky, U.S. Patent No. 5,418,174 and in further view of Wolf, Vol. 2.

The Examiner has asserted that the combination, of Williams, Kalnitsky and Wolf teaches the following (See Office Action dated August 18, 2003):

> Williams discloses a MOS gated device which is resistant to single event radiation failure and having improved total dose radiation resistance; said device comprising: a P-type substrate (10 20) having substantially flat, parallel upper (20) and lower (10) surfaces; a plurality of laterally spaced N-type body regions (82 40) extending from said upper surface into said substrate (20); at least one respective P-type source region (84) formed in each of said body regions (82) in said upper surface of said substrate (20) and defining a respective channel region (40) in said upper surface in said body region; a gate electrode (60) comprised p-type silicon including boron dopants (see Col. 2, lines 51-60) disposed atop and insulated from said channel region and operable to invert said channel region in response to the application of a suitable gate voltage to said gate electrode (60) and said gate (60) being insulated from said channel region (62) by a gate oxide layer (50) comprising silicon dioxide having a thickness of between 500 to 1000 angstroms; and a source electrode (84) disposed atop said first surface (20) and connected to each of said source regions (82); said gate electrode being comprised of P-type silicon; and an interlayer dielectric layer (6) formed atop gate electrode (60) and having openings (see Fig. 1) therein which said source drain regions (see Figs. 1-7) and also col. 2, lines 52-68 through col. 3, lines 1-7).
>
> However, Williams does not specifically disclose the gate oxide layer being radiation hardened.

Kalnitsky discloses semiconductor device that has a gate (16) being insulated from said channel region by a gate dioxide layer (14) and said gate dioxide layer being radiation hardened (see Fig. 1 and col. 1, lines 11-35). Kalnitsky discloses that "Ionizing radiation is known to produce defects in semiconductors. For example, radiation generates unwanted holes and electrons in gate oxides and other oxide dielectric layers. Throughout the dielectric, radiation generates electron-hole pairs. Some of these electron-hole pairs will recombine while others will not, yielding free electrons and holes. If an irradiated dielectric is a gate oxide, by applying a negative voltage to the gate electrode, the electrons will move toward the substrate and the holes will move toward the gate electrode. If a positive voltage is applied to the gate electrode, the reverse will occur, the electrons will move toward the gate electrode and the holes will move toward the substrate. This movement of and subsequent trapping of electrons and holes on intrinsic trapping sites causes a shift in the threshold voltage due to the radiation. Radiation ultimately induces a build up of positive charge within the dielectric due to large capture cross-sections of hole traps. Various methods have been employed to form radiation hard gate oxides to compensate for the build up of positive charges and to prevent such shifts in the threshold voltage from occurring when the integrated circuit or device is subjected to radiation." (see Kalnitsky, col. 1, lines 10-35).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to have provided Williams reference with radiation hardened gate oxide layer as taught by Kalnitsky because the process would have induced a build up of positive charge within the dielectric (i.e. gate oxide) due to large capture cross-sections of the traps the radiation hardened gate oxide layer and as result shifts in the threshold voltage would have been prevented from occurring when the integrated circuit or device is subjected to radiation.

In an Office Action dated April 29, 2004, the Examiner added the following comments regarding the cited references:

Williams, Kalnitsky and Wolf are applied as stated in the Office Action mailed 8/18/03 and as follows:

Williams discloses that the gate oxide 50 is grown typically in a dry thermal oxidation to a thickness of 100-1200 angstroms (col. 4, lines 38-40).

Wolf, pp. 207-210, newly cited, discloses dry oxidation at 800-1100°C (p. 208, 210) to produce gate oxides.

It would have been within the scope of one of ordinary skill in the art to employ the conditions of Wolf, Vol. 2, to enable the disclosed dry oxidation step

of Williams to be performed. In that event it is expected that the resulting device would exhibit the recited property with respect to the radiation hardness because the conditions would then be as disclosed to be so effective on instant page 14, especially after the radiation hardening step of Kalnitsky.

In an Office Action dated November 2, 2004, the Examiner further added the following comments:

> The rejection is maintained as stated in the paper mailed 4/29/04 and as follows.
>
> The device produced by the process of the combination of Williams in view of Kalnitsky and Wolf, Vol. 2 would exhibit the recited properties because the same materials would be treated in the same manner as in the instant invention disclosed on instant page 14, for example. Furthermore, the device would have the recited properties because the claim does not set forth the degree to which the device exhibits the properties.

VII. ARGUMENT

The Examiner's precise ground for rejection is not understood well. In the Office Action dated August 18, 2003, the Examiner appears to have stated that Williams teaches all of the limitations of claim 1, except that it does not teach a radiation hardened gate oxide, which, according to the Examiner is taught by Kalnitsky.

In the Office Action dated April 29, 2004, the Examiner refers to the prior grounds for rejection, but further states that Williams as modified by Wolf would have a gate oxide that is 1000Å or thinner, and radiation hardened "specially after the radiation hardening step of Kalnitsky."

In the Office Action dated November 2, 2004, the Examiner again refers to the prior grounds of rejection and then adds that a device modified according to the teachings of Williams, Kalnitsky and Wolf would have the same properties as the device in claim 1.

It is respectfully submitted that no matter what combination the Examiner uses claim 1 is not obvious in that a skilled person would not have expected the combination to result in a device according to claim 1.

The Examiner agrees that Williams does not show a radiation hardened gate oxide.

Kalnitsky fails to teach the use of a radiation hardened gate oxide that is less than 1000Å thick as called for by claim 1.

Wolf has been cited as an additional reference to illustrate that gate oxides can be produced by dry oxidation at 800-1100°C. Wolf, however, does not state that the gate oxides so produced can withstand damage due to total dose radiation as well as SEE, which is a key element of a device according to the present invention. Specifically, Wolf does not specify that a P-channel device can be modified to include a gate oxide that is less than 1000Å and can resist damage due to total does radiation as well as SEE.

The Examiner appears to conclude that if someone were to combine these references, the combination would be a device according to the present invention. However, there has to be a motivation or suggestion in the art compelling the skilled person to combine the references.

In this case the opposite is true. That is, the conventional thinking prior to the invention was that a radiation hardened gate oxide that is less than 1300Å thick cannot withstand SEE. Therefore, one skilled in the art would not have expected the Examiner's suggested combination to succeed. Specifically, the Examiner has stated that claim 1 is obvious presumably because a skilled person would modify a radiation hardened gate oxide as shown by Kalnitsky and reduce the thickness thereof according to Wolf in that Wolf teaches a range of thickness, which includes the claimed range. A skilled person could have only modified Kalnitsky if he/she expected the modification to yield the subject matter of claim 1. However, a skilled person at the time of the invention would not have expected the gate oxide to be able to withstand SEE. Thus, a skilled person would not have expected the Examiner's combination to succeed. It is respectfully submitted, therefore, that the combination of references set forth by the Examiner does render the subject matter of claim 1 obvious as it would not have been expected to result in a device according to claim 1.

In addition, the Examiner has concluded that Williams teaches all of the limitations of claim 1, including a gate oxide that is less than 1000Å thick and a gate electrode comprised of p-type polysilicon. In the previous papers filed, the applicants' attorneys maintained that Williams does not teach a p-type gate electrode in combination with a gate oxide that is less than 1000Å thick. That, in fact, Williams teaches away from such a combination. The following excerpt from Williams illustrates the latter point:

> "Another conventional technique for reducing V_{tp} of a PMOS device, one which is useful even in processes having long diffusion times after the polysilicon deposition step, is to use boron-doped p-type polysilicon gates in association with the PMOS devices, instead of phosphorus-doped n-type polysilicon gates. The p-type polysilicon has a different work function, so that the threshold of the PMOS devices is shifted by about a volt. Unfortunately, this technique is not entirely satisfactory for use in processes specifying a thin gate oxide, as the boron from the p-type polysilicon penetrates easily through the thin gate oxide in any subsequent diffusion steps and can counterdope the channel. Leakage and other problems result." (emphasis added).

Williams does not show a device with a p-type gate electrode and a gate oxide layer that is less than 1000Å thick. Williams mentions the 1000Å thick gate oxide only to explain that the combination of a p-type gate electrode and a gate oxide that is less than 1000Å thick leads to "unsatisfactory" results. Clearly, Williams is discouraging the use of a 1000Å thick gate oxide layer in combination with a p-type gate electrode. Thus, although Williams teaches that a MOSgated device having a p-type gate electrode is possible, it explicitly states that such a device should not have a gate oxide that is less than 1000Å thick. Col. 2, lines 65-68.

However, the Examiner states that Williams teaches using a gate oxide layer that is between 500-1000Å thick. Williams, however, teaches using 100-1200Å thick gate oxide layer in combination with an n-type gate electrode. Given the explicit statements in Williams to not combine a gate oxide layer that is less than 1000Å thick with a p-type gate electrode, it cannot be said that Williams teaches a device with a p-type gate electrode and a gate oxide that is less than 1000Å thick.

For this additional reason Williams cannot be modified to have a gate oxide that is less than 1000Å thick in combination with a P type gate electrode, which is the subject of claim 1.

Claims 3-7, 9 and 11-13 depend from claim 1, and, therefore, include at least its limitations. Each of these claims includes other limitations, which in combination with those of claim 1, are not shown or suggested by the art of record.

VIII. CONCLUSION

If this communication is filed after a shortened statutory time period has elapsed and no separate Petition is enclosed, the Commissioner of Patents and Trademarks is petitioned, under 37 C.F.R. §1.136(a), to extend the time for filing a response to the outstanding Office Action by the number of months which will avoid abandonment under 37 C.F.R. §1.135. The fee under 37 C.F.R. §1.17 should be charged to our Deposit Account No. 15-0700.

In the event the actual fee is greater than the payment submitted or is inadvertently not enclosed or if any additional fee during the prosecution of this application is not paid, the Patent Office is authorized to charge the underpayment to Deposit Account No. 15-0700.

EXPRESS MAIL CERTIFICATE

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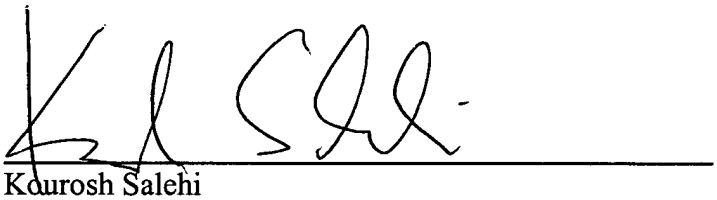
DOROTHY JENKINS
Name of Person Mailing Correspondence

Dorothy Jenkins
Signature

March 10, 2006
Date of Signature

KS:gl

Respectfully submitted,



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CLAIMS APPENDIX

1. A P-channel MOS gated device which is resistant to single event radiation failure and having improved total dose radiation resistance; said device comprising:

a P-type substrate having substantially flat, parallel upper and lower surfaces;

a plurality of laterally spaced N-type body regions extending from said upper surface into said substrate;

at least one respective P-type source region formed in each of said body regions in said upper surface of said substrate and defining a respective channel region in said upper surface in said N-type body region;

a gate electrode comprised of p-type polysilicon disposed atop and insulated from said channel region and operable to invert said channel region in response to the application of a suitable gate voltage to said gate electrode said gate being insulated from said channel region by a gate oxide layer comprising silicon dioxide, said gate oxide layer being comprised of radiation hardened silicon dioxide and less than 1000Å thick; and

a source electrode disposed atop said upper surface and connected to said at least one P-type source region;

wherein said gate oxide is capable of resisting threshold voltage shift due to total radiation dose and capable of resisting single event gate rupture due to a single event effect.

3. The MOS gated device of claim 2 wherein said gate dielectric has a thickness of between 500 to 1000Å.

4. The MOS gated device of claim 1 wherein each of said N-type channel regions has a doping concentration corresponding to that of an approximately 100 KeV phosphorus implant at a dose of about $5.5x10^{13}$ atoms/cm^2.

5. The MOS gated device of claim 1 wherein each of said N-type channel regions has a doping concentration corresponding to that of an approximately 100 KeV phosphorus implant at a dose of about $8.0x10^{13}$ atoms/cm^2.

6. The MOS gated device of claim 1 wherein said substrate includes a chip of monocrystalline silicon at said lower surface of said substrate and an epitaxial layer formed atop said chip and that is less heavily doped than said chip.

7. The MOS gated device of claim 1 wherein at least one of said N-type body regions includes a portion adjacent to said upper surface that is more heavily doped than another portion of said N-type body regions that is adjacent to a lower boundary between said N-type body region and said substrate.

9. The MOS gated device of claim 1 wherein said interlayer dielectric is low temperature oxide.

11. The MOS gated device of claim 1 further comprising a passivation layer formed atop said source electrode.

12. The MOS gated device of claim 11 wherein said passivation layer is comprised of low temperature oxide.

13. The MOS gated device of claim 1 wherein said gate electrode has a doping concentration corresponding to that of an approximately 50 KeV boron implant of about $5x10^{15}$ atoms/cm^2.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.